LOC 4700 DAE #9

Practitioner's Docket No. 00CXT0725N-1 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Duane E. Galbi
Application No.: 09/919,283 Group No.: 2666
Filed: 07/31/2001 Examiner: Robert C. Scheibel
For: METHOD FOR AUTOMATIC RESOURCE RESERVATION AND COMMUNICATION THAT FACILITATES USING MULTIPLE PROCESSING EVENTS FOR A SINGLE PROCESSING TASK

MAIL STOP: Office of Petitions
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

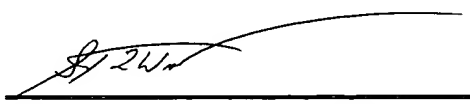
RENEWED PETITION UNDER 37CFR 1.78(a)(3) FOR UNINTENTIALLY DELAYED DOMESTIC PRIORITY CLAIM

The undersigned attorney of record hereby petitions to claim the benefit of the earlier filing date and cross-references to provisional application number 60/221,821; non-provisional application 09/639,915; non-provisional application 09/640,258; and non-provisional application 09/640,231. A substitute Amendment showing the relationship between the current application and the related application is included with this Renewed Petition.

The entire delay between the date the claim was due under paragraph (a)(5)(ii) of Section 1.78 and the date the claim was filed in the response to the Office Action was unintentional.

Applicant hereby encloses the USPTO credit card payment form for the surcharge set forth in Section 1.17(t).

Respectfully submitted,



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PTO/SB/21 (08-03)
Approved for use through 07/31/2006. OMB 0651-0031
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Application Number	09/919,283; Confirmation No. 2490
Filing Date	7/31/2001
First Named Inventor	Duane E. Galbi
Art Unit	2666
Examiner Name	Robert C. Scheibel
Total Number of Pages in This Submission: 15	Attorney Docket Number: 00CXT0725N-1

ENCLOSURES ***(check all that apply)***

- ☒ Fee Transmittal Form
  - ☒ Fee Attached
- ☒ Amendment / Reply
  - ☐ After Final
  - ☐ Affidavits/declaration(s)
- ☐ Extension of Time Request
- ☐ Express Abandonment Request
- ☐ Information Disclosure Statement
- ☐ Certified Copy of Priority Document(s)
- ☐ Response to Missing Parts/ Incomplete Application
  - ☐ Response to Missing Parts under 37 CFR 1.52 or 1.53
- ☐ Drawing(s)
- ☐ Licensing-related Papers
- ☒ Petition
- ☐ Petition to Convert to a Provisional Application
- ☐ Power of Attorney, Revocation Change of Correspondence Address
- ☐ Terminal Disclaimer
- ☐ Request for Refund
- ☐ CD, Number of CD(s) _____
- ☐ After Allowance Communication to Group
- ☐ Appeal Communication to Board of Appeals and Interferences
- ☐ Appeal Communication to Group **(Appeal Notice, Brief, Reply Brief)**
- ☐ Proprietary Information
- ☐ Status Letter
- ☐ Other Enclosure(s) *(please identify below)*:

Remarks

It is believed that no fees are due in this matter. However, if it is determined that fees are due, the Commissioner is authorized to debit Deposit Account No. 502622 for the required fees.

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm or Individual name	Steven L.Webb, Reg. 44,395
Signature	
Date	6/17/04

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being facsimile transmitted to the USPTO or deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date shown below.

Typed or printed name	Laura S. Mellblom		
Signature	Laura S. Mellblom	Date	6-17-04

#10

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Response to Dismissed Petition

This is in response to the Dismissed Petition dated June 2, 2004.

Amendment to the specification

Please amend the paragraph on page 1 entitled "related applications:" such that the results are as follows:

Related Applications:

1) The current non-provisional application claims priority from provisional ~~Application serial number~~ application 60/221,821 entitled "Traffic Stream Processor" filed on July 31, 2000 which is hereby incorporated by reference.

2) The current application is a continuation of the non-provisional ~~Application serial number~~ application 09/639,915 entitled "Integrated Circuit that Processes Communication Packets with Scheduler Circuitry that Executes Scheduling Algorithms based on Cached Scheduling Parameters" filed on August 16, 2000 which is hereby incorporated by reference and which claims priority of the provisional application number 60/149,379 filed on 8/17,1999 entitled "High speed communication processing device for internet protocol, asynchronous transfer mode, frame relay, and sonnet communications".

3) The current application is a continuation of the non-provisional ~~Application serial number~~ application 09/640,258 entitled "Integrated Circuit that Processes Communication Packets with Co-Processor Circuitry to Determine a Prioritized Processing Order for a Core Processor" filed on August 16, 2000 which is hereby incorporated by reference and which claims priority of the provisional application number 60/149,379 filed on 8/17,1999 entitled "High speed communication processing device for internet protocol, asynchronous transfer mode, frame relay, and sonnet communications".

4) The current application is a continuation of the non-provisional ~~Application serial number~~ application 09/640,231 entitled "Integrated Circuit that Processes Communication Packets with Co-Processor Circuitry to Correlate a Packet Stream with Context Information" filed on August 16, 2000 which is hereby incorporated by reference and which claims priority of the provisional application number 60/149,379 filed on

8/17,1999 entitled "High speed communication processing device for internet protocol, asynchronous transfer mode, frame relay, and sonnet communications".

~~The content of the above applications is hereby incorporated herein by reference.~~

Please amend the paragraph starting on line 18 of page 10 such that the results are:

In operation, receive interface 106 receives new packets from communication system 101, and scheduler 105 initiates transmissions of previously received packets that are typically stored in memory 103. To initiate packet handling, receive interface 106 and scheduler 105 transfer requests to co-processor circuitry 107. Under software control, core processor 104 may also request packet handling from co-processor circuitry 107. Co-processor circuitry 107 fields the requests, correlates the packets with their respective context information, and creates a prioritized work queue for core processor 104. Core processor 104 processes the packets and context information in order from the prioritized work queue. Advantageously, co-processor circuitry 107 operates in parallel with core processor 104 to offload the context correlation and prioritization tasks to conserve important core processing capacity. ~~In response to packet handling, core processor 104 typically initiates packet transfers to either memory 103 or communication system 102. If the packet is transferred to memory 103, then core processor instructs scheduler 105 to schedule and initiate future packet transmission or processing. Advantageously, scheduler 105 operates in parallel with core processor 104 to offload scheduling tasks and conserve important core processing capacity.~~

In response to packet handling, core processor 104 typically initiates packet transfers to either memory 103 or communication system 102. If the packet is transferred to memory 103, then core processor 104 instructs scheduler 105 to schedule and initiate future packet transmission or processing. Advantageously, scheduler 105 operates in parallel with core processor 104 to offload scheduling tasks and conserve important core processing capacity.

Please amend the paragraph starting on line 1 of page 28 such that the results are:

The system is setup so that if step 922 is delayed by stalls in the system such that this event request is really processed after 912 happens, the data buffer is reserved using in-use counts by the 921 operation until the 922 operation can take place. This assures that independent of the relative timing of 922 and 912 this is not time between 912 and 922 that the value of the data buffer's in-use count allows this passed data buffer to be viewed as an unassigned data buffer. The effective reservation of this data buffer by incrementing the <u>in</u> ~~is~~-use count when the event request 921 is posted, assures that no intervening event request can mistakenly view this data buffer as unassigned and reallocate this data buffer

Amendments to the Claims

Please amend the claims such that the results are:

1. (Original) An integrated circuit for processing events related to communication packets, said integrated circuit comprising:

a core processor configured to execute software to process a series of communication packets, the processing of each packet being an event and having associated data and context information; and

a co-processor comprising a plurality of state information buffers for storing state information associated with events wherein each of said state information buffers having an in-use counter indicating the number of events associated with the contents of said buffer.

2. (Original) The integrated circuit of claim 1 wherein said co-processor comprises a plurality of context buffers for storing context information associated with a plurality of events.

3. (Original) The integrated circuit of claim 2 wherein said co-processor comprises an in-use counter associated with each of said context buffers.

4. (Original) The integrated circuit of claim 1 wherein said co-processor comprises a plurality of data buffers for storing data.

5. (Original) The integrated circuit of claim 4 wherein said co-processor comprises an in-use counter associated with each of said data buffers.

6. (Original) The integrated circuit of claim 1 wherein said integrated circuit comprises a plurality of data buffers each having an in-use counter whereby data can be transferred from one event to another event by changing information in a data buffer.

7. (Original) The integrated circuit of claim 1 wherein said integrated circuit comprises a plurality of buffers for data associated with events and a plurality of buffers for context associated with events.

8. (Original) The integrated circuit of claim 7 wherein said integrated circuit comprises an in-use counter associated with each of said buffers.

9. (Original) The integrated circuit of claim 1 wherein said co-processor comprises a plurality of data only information buffers, a plurality of context information buffers, an in-use counter for each of said data only buffers and an in-use counter for each of said context buffers.

10. (Original) The integrated circuit of claim 9 where data can be passed from one event to another event by changing the data in one of said state information buffers.

11. (Original) A method of processing events related to communication packets in an integrated circuit which includes a core processor and a co-processor having a state information buffer for storing state information for an event separate from the data associated with said event, said state information buffer having an associated in use counter, the method comprising:

incrementing the in-use counter associated with said state information buffer when an event is associated with said state information buffer; and

decrementing the in-use counter of said state information buffer when said event associated with said buffer is finished.

12. (Original) The method of claim 11 wherein said integrated circuit comprises a plurality of state information buffers.

13. (Original) The method of claim 11 wherein said integrated circuit comprises a context buffer and an in-use counter for said context information buffer and the method further comprises:

incrementing the in-use counter associated with said context buffer when an event is associated with said context buffer; and

decrementing the in-use counter of said context buffer when said events associated with said context buffer is finished.

14. (Original) The method of claim 11 wherein said integrated circuit comprises a data only buffer to store data associated with an event.

15. (Original) The method of claim 11 wherein said integrated circuit comprises a data only buffer to store data associated with an event and an in-use counter associated with said data only buffer and the method further comprises:

incrementing the in-use counter associated with said data buffer when an event is associated with said data buffer; and

decrementing the in-use counter of said data buffer when said event associated with said data buffer is finished.

16. (Original) An integrated circuit for processing events associated with communication packets which includes a core processor and a co-processor, the improvement which comprises, separate buffers for data and state information and in-use counters for all of said buffers, whereby the contents of a data can be passed from one event to another event, each of said events having state information in a separate state information buffer.

17. (Original) The integrated circuit of claim 16 which includes context information buffers.

18. (Original) The integrated circuit of claim 17 which includes in-use counters for said context information buffers.

19. (Original) The integrated circuit of claim 16 including a plurality of data buffers and a plurality of state information buffers.

20. (Currently amended) The integrated circuit of claim 16 which includes a plurality of data buffers, a plurality of state information buffers and a plurality of context information buffers, each of said plurality of data buffers and each of said plurality of state information buffers and each of said plurality of context buffers having an in-use counter which is ~~increments~~ incremented when an event is associated with ~~the~~ one of the plurality of data buffers or with one of the plurality of state information buffers or with one of said plurality of context buffers and decremented when an event is finished utilizing ~~the~~ one of the plurality of data buffers or with one of the plurality of state information buffers or with one of said plurality of context buffer.

21. (Original) An integrated circuit for processing events related to communication packets, said integrated circuit comprising:

a core processor configured to execute software to process a series of communication packets, the processing of each packet being an event and having associated data, state and context information; and

a co-processor having a plurality buffers which separately store data, state and context information associated with events wherein each of said data, state and context buffers having an in-use counter indicating the number of events associated with said buffer.

Remarks

The related application paragraph in the specification has been amended to include the relationship between the current application and the related applications and to fix the incorporation by reference of 60/149,379. A renewed petition for an unintentionally delayed benefit claim is included in this reply.

The Claims 1 – 21 are pending and rejected. Applicants traverses the rejection of claims 1 – 21 and requests allowance of claims 1 – 21.

The specification has been amended to correct the informalities noted by the examiner.

Claim 20 is objected to because the phrase "is increments" on line 4 is incorrect. Claim 20 has been amended to correct for this informality.

Claims 16 and 20 are rejected under 35 UNC 112, second paragraph, as being indefinite. The examiner objected to the phrase "the improvement" in line 3 of claim 16. Claim 16 is a Jepson type claim and the phrase "the improvement which comprises" is the transition phrase (see 37 CFR 1.75(e)). Claim 20 has been amended to correct the antecedent basis problem.

Claim 1 has been rejected under 35 U.S.C. 103(a) as being unpatentable over US 6,373,846 to Daniel et. al. in view of US 5,896,511 to Manning et. al. The prior art reference (or references when combined) must teach or suggest all the claim limitations. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). Claim 1 has the limitation for "a co-processor comprising a plurality of state information buffers for storing state information associated with events wherein each of said state information buffers having an in-use counter indicating the number of events associated with the contents of said buffer". The state information stored in the state information buffers "includes a data buffer pointer, a context pointer, context validity bit, requester indicator, port status, a channel descriptor loaded indicator" (see page 13, lines 22 – 25). In addition to the state information, the state information buffers store an indication (a count) of the number of events the number of events associated with the contents of said buffer.

The buffers in Manning are not state information buffers and do not store state information associated with events. The buffers in Manning are counters. The counters store the number of buffers being used in a link or connection between two processors on

different chips in different devices. For example "Link_Buffer_Counter 62 provides an indication of the number of buffers in the downstream element which are currently being used by all connections..." (see column 10, lines 6 – 10). The counters in Manning do not store any state information as required by claim 1. Furthermore, the buffers in Manning are not in the co-processor, the buffers in manning are implemented in external RAM associated with the FSPP processor (see column 9, lines 44 – 46). Because the buffers in Manning are external to the co-processor and do not store state information in addition to a count, the examiner has not established the requirements for a *prima facie* case for obviousness and claim 1 is allowable as written.

Claims 2 – 10 depend on allowable claim 1. If an independent claim is nonobvious under 35 U.S.C. 103, then any claim dependent therefrom is nonobvious. *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988). Therefore claims 2 – 10 are also allowable.

Claim 11 has been rejected under 35 U.S.C. 103(a) as being unpatentable over US 6,373,846 to Daniel et. al. in view of US 5,896,511 to Manning et. al. Claim 11 has the limitation of a co-processor having state information buffers for storing state information and having an associated in use counter for the state information buffers. Therefore the arguments for claim 1 (above) apply to claim 11. Therefore claim 11 is allowable as written.

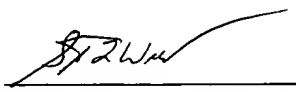
Claims 12 – 15 depend on allowable claim 11. Therefore claims 12 – 15 are also allowable.

Claim 16 has been rejected under 35 U.S.C. 103(a) as being unpatentable over US 6,373,846 to Daniel et. al. in view of US 5,896,511 to Manning et. al. and in further view of US 6,310,879 to Zhou et. al. Claim 16 contains the requirement for state information buffers with an in-use counter. Zhou does not teach state information buffers with in use counters. As described for claim 1 (above) Manning does not contain state information buffers with in use counters. Therefore claim 16 is allowable as written.

Claims 17 – 20 depend on allowable claim 16 and are therefore allowable.

Claim 21 has the limitation for a co-processor having buffers to store state information where the state information buffers have an in use counter. The arguments for claim 16 (above) therefore apply to claim 21 and claim 21 is allowable as written.

This application is now considered to be in condition for allowance and applicants respectfully request allowance of claims 1 – 21.



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